PATENT APPLICATION
DOCKET NO.: 1263-0025US

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

Claims 1 - 8. (Canceled)

9. (Currently Amended) A Static Random Access Memory (SRAM) instance, comprising:

a plurality of SRAM cells organized in an array having rows and columns, each SRAM cell including a pair of cross-coupled inverters that are coupled to form a pair of data nodes, wherein pull-down devices of said SRAM cells forming a row are coupled together to be biased by a bias potential in standby mode;

a row decoder for selectively activating wordlines based on a decoded address, wherein each wordline is operable to drive a corresponding row of said array; and

a multiplexer disposed between said row decoder and said array for deactivating said bias potential provided to said SRAM cells of a particular row when said particular row is driven by a wordline associated therewith, wherein said multiplexer includes a plurality of bias switch elements, each corresponding to a wordline, said each bias switch element comprising logic circuitry driven by a

corresponding wordline to deactivate said bias potential when said corresponding wordline is driven high.

10. (Original) The SRAM instance as set forth in claim 9, wherein said decoded address comprises a row address.

11. (Original) The SRAM instance as set forth in claim 9, wherein said pull-down devices of said SRAM cells comprise N-channel field-effect transistor (N-FET) devices.

12. (Original) The SRAM instance as set forth in claim 9, wherein said bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts.

13. (Original) The SRAM instance as set forth in claim 9, wherein said bias potential is operable to preserve stability of logic levels stored at said data nodes of an SRAM cell.

Claims 14 and 15. (Canceled)

16. (Original) The SRAM instance as set forth in claim 9, wherein said bias potential is applied by biasing a body well potential of said pull-down device.

17. (Original) The SRAM instance as set forth in claim 9, wherein said bias potential is selected to preserve stability of said SRAM cells.

18. (Original) The SRAM instance as set forth in claim 9, wherein said bias potential is applied by biasing said pull-down devices' respective source terminals.

19. (Currently Amended) A memory compiler for compiling at least one Static Random Access Memory (SRAM) memory instance, comprising:

a code portion for generating a plurality of SRAM memory cells organized in an array having rows and columns, each SRAM cell including a pair of cross-coupled inverters that are coupled to form a pair of data nodes, wherein pull-down devices of said SRAM cells forming a row are coupled together to be biased by a bias potential in standby mode;

a code portion for generating a row decoder that selectively activates wordlines based on a decoded address, wherein each wordline is operable to drive a corresponding row of said array; and

a code portion for generating a multiplexer disposed between said row decoder and said array, said multiplexer for deactivating said bias potential provided to said SRAM cells of a particular row when said particular row is driven by a wordline associated therewith, wherein said multiplexer includes a plurality of bias switch elements, each corresponding to a wordline, said each bias switch element comprising logic circuitry driven by a corresponding wordline to deactivate said bias potential when said corresponding wordline is driven high.

20. (Original) The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said decoded address comprises a row address.

21. (Original) The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said pull-down devices of said SRAM cells comprise N-channel field-effect transistor (N-FET) devices.

22. (Original) The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts.

23. (Original) The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is operable to preserve stability of logic levels stored at said data nodes of an SRAM cell.

Claims 24 and 25. (Canceled)

26. (Original) The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is applied by biasing a body well potential of said pull-down device.

27. (Original) The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is selected to preserve stability of said SRAM cells.

28. (Original) The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is applied by biasing said pull-down devices' respective source terminals.

29. (Currently Amended) A memory operation method associated with a Static Random Access Memory (SRAM) instance, said SRAM instance having a plurality of SRAM memory cells organized in an array having rows and columns, each SRAM cell including a pair of cross-coupled inverters that are coupled to form a pair of data nodes, comprising:

in standby mode, providing a bias potential to pull-down devices of said SRAM cells that form a row of said array;

selectively activating a wordline based on a decoded address for a memory read operation, said wordline for accessing a bitcell on a row of SRAM cells; [[and]]

responsive to activating said wordline, deactivating said bias potential from said pull-down devices of said row of SRAM cells;

selecting a particular bitline column based on a column address;

reading a data value stored at a select bitcell selected by said row address and said column address while continuing to activate said bias potential of remaining bitcells of said particular bitline column; and

upon completion of said reading, re-activating said bias potential to said row of SRAM cells associated with said row address.

30. (Original) The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said decoded address comprises a row address.

Claim 31. (Canceled)

32. (Currently Amended) The memory operation method associated with an SRAM instance as set forth in claim [[31]] 29, wherein said bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts.

Claim 33. (Canceled)

34. (Original) The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said bias potential is applied by biasing a body well potential of said pull-down device.

35. (Original) The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said bias potential is selected to preserve stability of said SRAM cells.

36. (Original) The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said bias potential is applied by biasing said pull-down devices' respective source terminals.

37. (New) A Static Random Access Memory (SRAM) circuit, comprising:

a plurality of SRAM cells organized in an array having rows and columns, wherein pull-down devices of said SRAM cells forming a row are biased by a bias potential; and

a plurality of bias switch elements, each corresponding to a wordline associated with a row of said array, said each bias switch element comprising logic circuitry driven by a corresponding wordline to deactivate said bias potential when said corresponding wordline is driven high.

38. (New) The SRAM circuit as set forth in claim 37, wherein said plurality of bias switch elements form a multiplexer disposed between said array and a row decoder, said row decoder for selectively activating wordlines based on a decoded row address, wherein each wordline is operable to drive a corresponding row of said array.

39. (New) The SRAM circuit as set forth in claim 37, wherein said pull-down devices of said SRAM cells comprise N-channel field-effect transistor (N-FET) devices.

40. (New) The SRAM circuit as set forth in claim 37, wherein said bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts.

41. (New) The SRAM circuit as set forth in claim 37, wherein said bias potential is operable to preserve stability of logic levels stored at data nodes of an SRAM cell.

42. (New) The SRAM circuit as set forth in claim 37, wherein said bias potential is applied by biasing a body well potential of said pull-down device.

43. (New) The SRAM circuit as set forth in claim 37, wherein said bias potential is selected to preserve stability of said SRAM cells.

44. (New) The SRAM circuit as set forth in claim 37, wherein said bias potential is applied by biasing said pull-down devices' respective source terminals.